PROJECT PROFILE

2A714: Hardware-dependent software for systems-on-chip (SoftSoC)

EDA FOR SOC DESIGN AND DFM

Partners:

CEA
Compaan Design
DS2
NXP Semiconductors
Thales
Thomson Grass Valley
TIMA-INPG
Uni Delft (TU Delft)
Uni Leiden (LIACS)
Virage Logic

Project leader:

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Key project dates:

Start: June 2008
End: May 2011

Countries involved:

France
Spain
The Netherlands

The primary objective of SoftSoC is to resolve the major productivity bottleneck in system-on-chip (SoC) design by developing systematic and highly-automated approaches to combining multiple hardware intellectual property with associated hardware-dependent software in efficient design packages. This involves separating operating-system and application software from the underlying hardware and hardware-dependent software for efficiency, dependability, flexibility and manageability. Solutions developed in this MEDEA+ project will enable Europe to maintain leadership in key strategic markets by increasing the capability of designers to build larger and better quality SoC devices more rapidly.

Most advanced consumer electronics products such as mobile phones, set-top-boxes (STBs) and digital televisions are based on system-on-chip (SoC) solutions consisting of a highly-integrated chip and associated software. Around 95% of SoCs combine hardware – function-specific components and accelerators – and programmable computing cores including central processing units (CPUs), digital signal processors and application-specific instruction set processors.

The integration of the hardware components in the SoC requires complementary software known as hardware-dependent software. Designing, building, configuring, integrating and testing software for advanced SoCs has become a huge task. The MEDEA+ 2A714 SoftSoC project aims to develop a highly-automated approach to improve the design process quality and productivity for ever more highly integrated SoCs.

SoftSoC is taking a pioneering approach to intellectual property (IP) integration for SoC design by separating the operating system and the application software from the underlying hardware and hardware-dependent software. The result should be significant improvements in design efficiency, workflow and overall process management.

Hardware-dependent software bridges the gap between specific hardware solutions that perform a certain function and hardware-independent application and middleware software. Target users of the SoftSoC solutions include major European chipmakers, fabless semiconductor suppliers and system design houses. The MEDEA+ project will deliver significant economic value to designers and chipmakers that adopt these solutions as the strategic and architectural foundation for future SoC design initiatives. SoftSoC will also enable a market place for hardware and software IP.

Simplifying SoC design reuse

In the last decade, several MEDEA+ projects have been initiated to increase productivity in the reuse of SoC designs and related IP. These projects encouraged the expansion of a strong European skill set that has helped create the present strength of Europe in several areas of complex systems design. The goal of SoftSoC is to capitalise on this expertise and expand it to the formalisation and automation of hardware/software integration. It will address multiprocessors and heterogeneous SoC design challenges such

as overall systems validation and optimisation, IP provisioning and management.

SoftSoC aims to solve the main productivity limitations confronting system designers when integrating new IP within existing CPU-based platforms. Such integration requires hardware-dependent software to drive the new IP. The process of developing this software is laborious and the debugging procedures very expensive. It is also very resource intensive to verify that the new IP functions correctly with the other parts of the platform. The project is, therefore, also addressing economic aspects of SoC design.

The solutions proposed will enable SoC designers to combine multiple hardware IP with their hardware-dependant software and the software associated with the programmable processors in more highly integrated SoCs. These can then be implemented and validated much more efficiently than when using traditional methods.

Application domains are extensive. Despite the fact that all large design houses are eagerly seeking efficient hardware/software integration solutions, no existing SoC has been designed using systematic and highly automated hardware/software integration methods. Industry is currently leaning towards more powerful heterogeneous SoCs able to handle both digital and analogue functions; the increasing complexity of managing the design process will drive widespread adoption of hardware-dependent software solutions.

Flexible generic architecture

The SoftSoC concept is based on a flexible generic architecture comprising a fixed computing infrastructure, with sufficient flexibility to embrace hardware and software IP specific to the application. Each IP will be based on three models – the hardware model, the hardware-dependent software required to control the IP and the test scenario for the IP.

These models will mitigate the IP integration problems and ensure the efficient validation of the IP and the system. At the same time, it will provide a drastic improvement in the SoC design process in terms of quality and productivity.

SoftSoC is based on four key planned innovations to bridge the gap between SoC applications and design methods:

1. Hardware/software formalisation, which covers overall validation and rationalisation of the complete system including both hardware and software components. Modelling innovations will consist of technology and standards for describing and packaging IP – hardware and hardware-dependent software – so making the IP easy to (re)use;
2. Exploiting the formalised models as integration technology will enable easy IP configuration, seamless composition and automated integration verification, reducing SoC design costs and time to market;
3. Tools that will support the architects, software developers and integrators in the application of the SoftSoC integration innovations. This is a key step in system design automation and architecture exploration; and
4. Standardisation efforts that will cover the hardware/software integration.

Boosting European leadership

The innovative solutions developed will enable Europe to maintain its current leadership position in this strategic market by increasing the capability of SoC designers to build larger and better quality systems in less time and with lower costs. The results will enable SoC designers to achieve significantly higher IP reuse by pooling common IP and breaking the 'one-application-to-one-IP' model.

Significant formalisation of hardware/software interfaces will reduce the overhead required to integrate new hardware IP. In addition, hardware-dependent software automation and IP-management solutions will reduce the time SoC designers have to spend on largely reactive tasks, such as provisioning, configuration, testing and debugging.

This MEDEA+ project will use several channels for exploitation of results. Systems and design house partners will use SoftSoC results for their internal needs, while the innovative SME partners will open up commercial channels. Furthermore, the concepts, methods, libraries and tools resulting from SoftSoC will be industrialised and marketed each time a profitable business scheme is proposed. Academic partners will use the findings to improve their education and research programmes.

Successful achievement of the goals of this MEDEA+ project will secure a leading position worldwide for Europe in the highly integrated SoC devices required especially in future communications, consumer electronics and automotive applications.

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MEDEA+ focuses on enabling technologies for the Information Society and aims to make Europe a leader in system innovation on silicon.